Notice of Allowability	Application No.	Applicant(s)	
	10/604,141	HASWELL ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview on 5/21/2007*.

2. ☒ The allowed claim(s) is/are *1-5,7-12 and 14-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *5/21/2007* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

5/24/07

GUY LAMARRE
PRIMARY EXAMINER

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with Peter Peterson on May 21, 2007.

Please replace the claims with:

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1. (Currently amended) A method of detecting error during transfer of data signals from a data memory to a computer processor comprising:

commencing transmission of a raw data signal and an error detection code for the raw data signal from a data memory to a computer processor, the computer processor operating on timed, uniform clock cycles;

at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for corruption based on its error detection code; and

if the data has not been corrupted, completing transmission of the raw data signal to the computer processor,

if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor;

processing the data signal with the computer processor,

wherein the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle.

2. (previously presented) The method of claim 1 wherein, if the error detection code indicates data corruption, further including determining if the corrupted data in the raw data signal may be corrected, and subsequently retrieving the corrected data and processing the corrected data signal with the computer processor.

3. (original) The method of claim 1 further including, if the computer processor processes the predetermined reserved signal, determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal and processing the corrected data signal with the computer processor.

4. (original) The method of claim 1 further including, if the corrupted data in the raw data signal has been corrected, replacing the raw data signal in the data memory with the corrected raw data signal.

5. (original) The method of claim 1 further including, if the computer processor processes a predetermined reserved signal, the computer processor executes an error handling routine comprising determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal, processing the corrected data signal with the computer processor, and replacing the raw data signal in the data memory with the corrected data signal.

6. (cancelled)

7. (original) The method of claim 1 further including commencing transmission of a subsequent raw data signal from the data memory to the computer processor and repeating the aforementioned steps for the subsequent raw data signal, until all desired raw data signals from the data memory are processed by the computer processor.

8. (original) The method of claim 1 wherein the raw data signal is a multi-bit data signal.

9. (original) The method of claim 1 wherein checking of the raw data signal for corruption by decoding the data and error detection code is performed simultaneously with the commencement of transmission of the raw data signal from the data memory to the computer processor.

10. (original) The method of claim 1 wherein the raw data signal is an instruction from a random access memory associated with the computer processor.

11. (currently amended) A system for detecting error during transfer of data signals from a data memory to a computer processor comprising:

a computer processor having a clock, the computer processor adapted to operate on timed, uniform clock cycles produced by the clock;

a data memory device containing raw data and an error detection code for the raw data to be processed by the computer processor, the raw data being in the form of a raw data signal;

a data checker device adapted to check the raw data for corruption and, if the error detection code indicates data corruption, correcting the corrupted data in the raw data; and

a computer processor instruction unit, the instruction unit adapted to commence transmission of a raw data from the data memory device to the computer processor and cause the data checker device to check the raw data signal for corruption, the instruction unit further adapted to cause completion of transmission of the raw data to the computer processor if the error detection code indicates no data corruption or, if the error detection code indicates data corruption, cause substitution of the raw data with a predetermined reserved instruction and transmission of the predetermined reserved instruction to the computer processor,

wherein the computer processor instruction unit is adapted to cause transmission of the raw data from the data memory device to the computer processor, the data checker device is

adapted to check simultaneously the raw data for presence of corruption, and the computer processor instruction unit is adapted to transmit either the raw data or predetermined reserved instruction to the computer processor, within a clock cycle.

12. (original) The system of claim 11 wherein the computer processor, upon processing a predetermined reserved instruction, is further adapted to execute an error handling routine comprising determining whether corrupted data in the raw data has been corrected, and, if corrected, retrieving the corrected data, processing the corrected data with the computer processor, and replacing the raw data in the data memory device with corrected data.

13. (cancelled)

14. (original) The system of claim 11 further including a corrected data register adapted to receive data corrected by the data checker device and transmit corrected data to the computer processor.

15. (original) The system of claim 11 wherein the data memory device is a random access memory associated with the computer processor and the raw data is an instruction from the random access memory for the computer processor.

16. (currently amended) A program storage device readable by a machine, embodying a program of instructions executable by the machine to perform method steps for detecting error

during transfer of a raw data signal and an error detection code for the raw data signal from a data memory to a computer processor, the computer processor operating on timed, uniform clock cycles, the raw data signal including an error detection code, the method comprising:

at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for corruption;

if the error detection code indicates no data corruption, completing transmission of the raw data signal to the computer processor,

if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor;

processing the data signal with the computer processor,

wherein the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle.

17. (previously presented) The program storage device of claim 16 wherein, if the error detection code indicates data corruption, the method further includes determining if the corrupted data in the raw data signal may be corrected, and subsequently retrieving the corrected data and processing the corrected data signal with the computer processor.

18. (original) The program storage device of claim 16 wherein the method further includes, if the computer processor processes the predetermined reserved instruction, determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal and processing the corrected data signal with the computer processor.

19. (original) The program storage device of claim 16 wherein the method further includes, if the corrupted data in the raw data signal has been corrected, replacing the raw data signal in the data memory with the corrected data signal.

20. (original) The program storage device of claim 16 wherein the error detection code comprises ECC code, and the raw data signal is an instruction from a random access memory associated with the computer processor.

REASONS FOR ALLOWANCE

Claims 1-5, 7-12 and 14-20 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches, for example, a method of detecting error during transfer of data signals from a data memory to a computer processor comprising: commencing transmission of a raw data signal and an error detection code for the raw data signal from a data memory to a computer processor, the computer processor operating on timed, uniform clock cycles; at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for

corruption based on its error detection code; and if the data has not been corrupted, completing transmission of the raw data signal to the computer processor, if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor; processing the data signal with the computer processor, wherein the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle. The foregoing limitations are not found in the prior arts of record. Particularly, none of the prior arts of record fully teach nor fairly suggest, "...commencing transmission of a raw data signal and an error detection code for the raw data signal from a data memory to a computer processor, the computer processor operating on timed, uniform clock cycles; at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for corruption based on its error detection code; and if the data has not been corrupted, completing transmission of the raw data signal to the computer processor, if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor; processing the data signal with the computer processor, wherein the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle."

Independent claims 11 and 16 include similar limitations of independent claim 1 and therefore are allowed for similar reasons.

Dependent claims 2-5, 7-10, 12, 14, 15 and 17-20 depend from allowable independent claims 1, 11 and 16 and inherently include limitations therein and therefore are allowed as well.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Fri 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2112
May 21, 2007

GUY LAMARRE
PRIMARY EXAMINER